FEB 16 2007
PATENT & TRADEMARK OFFICE

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Koos et al.

Attorney Docket No.: NOVLP068/NVLS-2818

Application No.: 10/690,084

Examiner: Vinh, Lan

Filed: October 20, 2003

Group: 1765

Title: METHOD FOR FABRICATION OF SEMICONDUCTOR INTERCONNECT STRUCTURE WITH REDUCED CAPACITANCE, LEAKAGE CURRENT, AND IMPROVED BREAKDOWN VOLTAGE

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on February 13, 2007 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: Chereyce Brown

Chereyce Brown

INFORMATION DISCLOSURE STATEMENT BEFORE FINAL ACTION OR NOTICE OF ALLOWANCE (37 CFR §§ 1.56 AND 1.97(c))

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449, a copy of which is attached, may be material to examination of the above-identified patent application. Applicants submit this reference in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make this citation of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that this reference indeed constitutes prior art.

02/20/2007 AWONDAF1 00000085 10690084
01 FC:1806 180.00 OP

This Information Disclosure Statement is being filed after the mailing date of the first Office Action on the merits, or after three months of the filing date of this application, whichever event occurred last, but it is believed before the mailing date of either: (i) a final action under

§1.113 or (ii) a notice of allowance under §1.311, whichever occurs first.

Accompanying this Information Disclosure Statement is

☐ a statement as specified in 37 CFR 1.97(e); or

☒ the fee set forth in 37 CFR 1.17(p).

If fees are due, enclosed is our Check No. 13277 for $180.00 in payment of the Information Disclosure Statement Fee. If it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NOVLP068).

Respectfully submitted,
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Form 1449 (Modified)	Atty Docket No.	Application No.:
	NOVLP068/NVLS-2818	10/690,084
Information Disclosure Statement By Applicant	Applicant: Koos et al.	
	Filing Date	Group
(Use Several Sheets if Necessary)	October 20, 2003	1765

U.S. Patent and Publication Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A1	7,008,871	03/2006	Andricacos et al.			
	A2	5,913,147	06/1999	Dubin et al.			
	A3	6,136,707	10/2000	Cohen			
	A4	5,891,513	04/1999	Dubin et al.			
	A5	6,065,424	05/2000	Shacham-Diamond et al.			
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	A7	5,972,192	10/1999	Dubin et al.			
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	A22	6,887,776	05/2005	Shang et al.			
	A23	2006/0205204	09/2006	Beck			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	B1	99/47731	09/23/99	WIPO			X	
Examiner				Date Considered				

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449 (Modified) **Information Disclosure Statement By Applicant** (Use Several Sheets if Necessary)	Atty Docket No. NOVLP068/NVLS-2818 Applicant: Koos et al. Filing Date October 20, 2003	Application No.: 10/690,084 Group 1765

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C1	U.S. Office Action mailed January 23, 2007, from U.S. Application No. 11/251,353. [Atty. Dkt. No. NOVLP141/NVLS-3107]
	C2	Andryuschenko et al., "Electroless and Electrolytic Seed Repair Effects on Damascene Feature Fill," Proceedings of International Interconnect Tech. Conf., San Francisco Ca., June 4-6, 2001, pp 33-35
	C3	Chen et al., "ECD Seed Layer for Inlaid Copper Metallisation," Semiconductor Fabtech – 12th Edition, 5 Pages, July 2000.
	C4	Ken M. Takahashi, "Electroplating Copper into Resistive Barrier Films," Journal of the Electrochemical Society, 147 (4) 1417-1417 (2000)
	C5	T.P. Moffat et al., "Superconformal Electrodeposition of Copper in 500-90 nm Features," Journal of the Electrochemical Society, 147 (12) 4524-4535 (2000)
	C6	Ritzdorf et al., "Electrochemically Deposited Copper," Conference Proceedings ULSI XV 2000, Materials Research Society, 101-107
	C7	Reid et al., "Optimization of Damascene Feature Fill for Copper Electroplating Process," Shipley Company, IITC 1999, 3 Pages
	C8	Reid et al., "Copper PVD and Electroplating," Solid State Technology, July 2000, www.solid-state.com, 86-103
	C9	Reid et al., "Factors Influencing Fill of IC Features Using Electroplated Copper," Adv Met Conf Proc 1999, MRS 10 Pages, (2000)
	C10	Shacham-Diamond et al., "Copper Electroless Deposition Technology for Ultr-Large-Scale-Integration (ULSI) Metallization," Microelectronic Engineering 33 (1997) 47-58
	C11	Hu et al., "Effects of Overlayers on Electromigration Reliability Improvement for Cu/Low K Interconnects," Presented in the Proceedings of the 42nd Annual IRPS held April 25-29, 2004, page v, article published May 28, 2004, 7 Pages.
	C12	Park et al., "Electroless Layer Plating Process and Apparatus", Novellus Systems, Inc., Application No. 10/235,420, filed September 30, 2002 [Atty. Dkt. No. NOVLP049/NVLS-2677]
	C13	U.S. Office Action dated September 1, 2005 for Application No. 10/235,420 [Atty. Dkt. No. NOVLP049/NVLS-2677]

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.